Research on Synchronization and Triggering of LXI Bus

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KEYWORDS

Synchronization; Triggering; Trigger response times; Trigger output response times; LXI triggering interface

ABSTRACT

With the development of the LXI technology, synchronization and triggering of LXI instruments has become hot topics in the research world. This paper analyzes five modes of LXI triggering. Combined with Trigger Response Times and Trigger Output Response Times mentioned in LXI Device Specification (Revision1.4), it elaborates the significance of LXI instruments synchronization via LXI Class A and Class B instrument synchronization accuracy test. Besides, taking LXI A logic analyzer for example, it introduces the implementation of LXI trigger interface in detail. According to the result of the LXI instrument clock synchronization experiment, the instruments can synchronize to each other with good precision.

Introduction

Since the founding of the LXI Consortium (Thorpe, 2011) in 2004, the development of LXI Instruments has caught more and more attention in test field. Currently, variety of universal and specific LXI Instruments, which have been widely applied to different fields (Sarfi, 2008; Proft and Lean, 2008; Qin and Qiu, 2010; Proft, 2007), have spring up and it can be up to 300 varieties. Besides, the development technique of LXI Instrument is tending to be mature, and the LXI Device Specification has also upgraded to Revision 1.4 (LXI, 2011). The reliability of LXI Instruments is also focused on (Peng, *et al.*, 2013; Wang, *et al.*, 2010).

There are three different classes (Sarfi, 2008) of LXI Instruments available: Class A, B and C. The main difference among them lies in the means to implement synchronization and triggering. Class C only includes LAN triggering and it can achieve millisecond-level precision; Class B that features with IEEE 1588 clock synchronization and time-based triggering could achieve microsecond-level precision; Class A features with LXI hardware bus triggering and its time precision can be up to nanosecond level. By comparison, it can be seen that Class C has a low time precision for synchronization, and there are few relevant researches on it. Contrarily, most attention is focused on IEEE 1588 Clock Synchronization that is included in Class A and B in different fields. Reference (Ken, 2008) mainly discusses some methods to improve the precision of IEEE 1588 Clock Synchronization in the field of industrial automation, while Jiho and Deogkyoon (Jiho and Deog-Kyoon, 2010) focuses on the application of IEEE1588-2008 in distributed control and test system. References (Zarick, *et al*., 2010; Jae and Jin, 2011; Schriegel and Kirschberger, 2010) mainly analyze implementation methods of IEEE 1588 from different aspects, including software, hardware and algorithm. All the references mentioned above mainly study the IEEE1588 Protocol, however, for LXI instruments; the IEEE 1588 Protocol has just taken the clock timing synchronization of two LXI instruments into consideration, ignoring the delay between timing trigger and signal generation (or acquisition). The delay ranges from several nanoseconds to hundreds of microseconds. Obviously, the delay will seriously influence the synchronization of LXI Class A and B instruments, which require microsecond-level or higher precision. Similarly,

for the synchronization and triggering of LXI Class A instruments, many researches attaches more importance to the implementation of hardware bus triggering (e.g. (Schriegel and Kirschberger, 2010; Li and Zhou, 2009)) than the synchronization of LXI Class A instruments. Based on the present situation, the paper conducts a deep research on LXI instruments' synchronization and triggering. Combined with the experience in developing LXI Class A Logic Analyzer, LXI Class B Multimeter, Oscilloscope and Arbitrary Waveform Generator (AWG) in Electronic Testing Technology and Instruments of the Ministry of Education Engineering Research Center in UESTC, it discusses LXI instruments triggering techniques and points out the significance of LXI instruments synchronization with the concepts of Trigger Response Times and Trigger Output Response Times that are put forward in the Revision 1.4 of LXI Device Specification (LXI, 2011).

Lxi Instruments Triggering

As referred in Section 3.1 of the LXI Device Specification Revision 1.4, LXI supports five modes of triggering: Driver command-based, Direct LXI Event Messaging, Time-based events, LXI Wired Trigger Bus-based and Optional vendor-specific hardware triggers.

(1) Command-based triggering

The implementation of this kind triggering mechanism is to send commands to instruments directly via the driver interface of the host PC. The most intuitive approach is to send commands via Agilent I/O Library to control instruments as shown in fig.1.

Commands for controlling instruments must belong to SCPI, and they can be the IEEE 488.2 command or vendor-specified.

For the development of LXI instruments, controlling instruments via commands is by the implementation of the VXI-11 and TCP/IP protocols. According to VXI-11 Protocol, some functions, such as creat_link, device_write, shall be implemented by the RPC techniques. The implementation of these functions establishes network channels for instruments, and instruments can be identified through Agilent I/O Libraries sending commands.

(2) Lxi Event Message Triggering

LXI Event Message Triggering is that LXI Devices can be triggered by LAN data packets between instruments. LAN data packet contains triggering information and the data format of it is specified in Section 3 of the LXI Device Specification Revision 1.4.

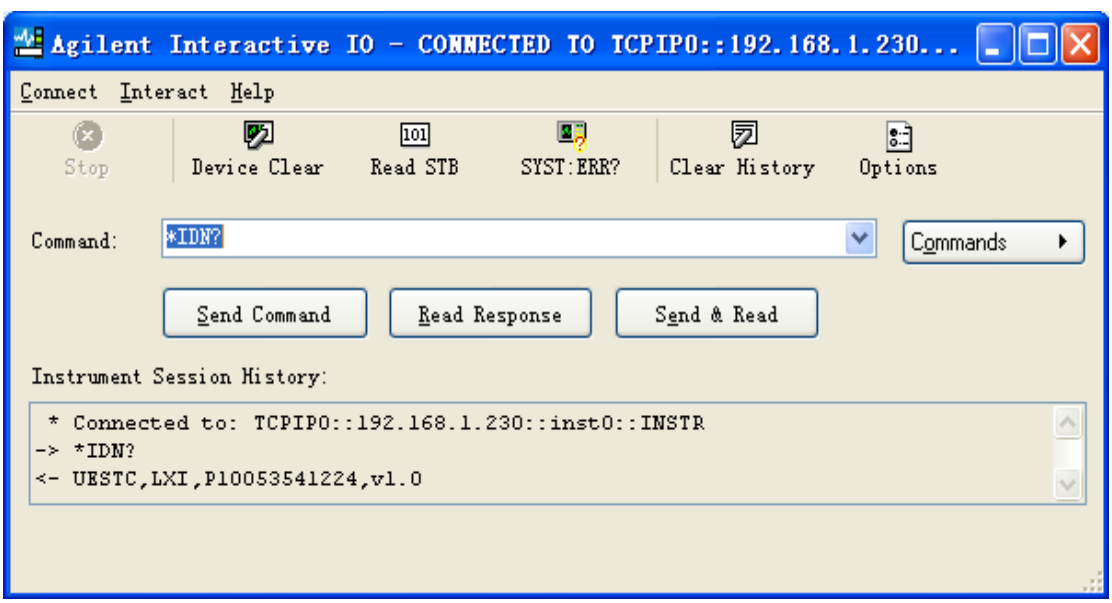

Figure 1: Send Commands Directly to Control Instruments via Agilent I/O Library.

(3) Time-Based Triggering using IEEE 1588
As is required in the LXI Device Specification, LXI Class A and B Devices should support the Time-based Triggering functionality using IEEE 1588. It's recommended that all LXI systems should include at least one module specially designed as highly stable clock and the clock should achieve 40 nanoseconds or better precision(refer to section 3.2 of the LXI Device Specification Revision 1.4 for more information). The time when triggers occur can be configured by the user and upon the arrival of triggering time, instruments will be triggered. If multiple LXI instruments are interconnected together as a test system via network, synchronization of all instruments in this system can be controlled by configuring the triggering the time of instruments. As shown in Fig. 2, two instruments need synchronous acquisition and the time of two instruments can be set to 08:000100 for synchronization. To ensure the two instruments to be triggered simultaneously; they both shall implement IEEE 1588 and synchronize periodically before being triggered.

(4) Lxi Hardware Bus Triggering
Similar to VXI and PXI Trigger Bus, LXI Class A devices can also transmit and receive trigger signals via LXI Hardware Trigger Bus, and it could achieve nanosecond-level precision. The LXI Wired Trigger Bus provides eight physically independent trigger channels LXI0-LXI7, and each channel is capable of operating in one of two modes: Driven mode and Wired-OR mode. In Driven Mode, only one LXI device has the privilege to control the LXI Wired Trigger Bus and send trigger signals to other LXI devices that can only receive trigger signals. Differently; in Wired-OR Mode, all LXI devices have the privilege to control the LXI Wired Trigger Bus and send trigger signals.

(5) Optional Vendor-Specific Hardware Triggering
Vendor-specified Triggering varies greatly in different LXI devices. Taking LXI Logic Analyzer for example, the Vendor-specified Triggering includes Sequence Triggering, Burr triggering and so on.

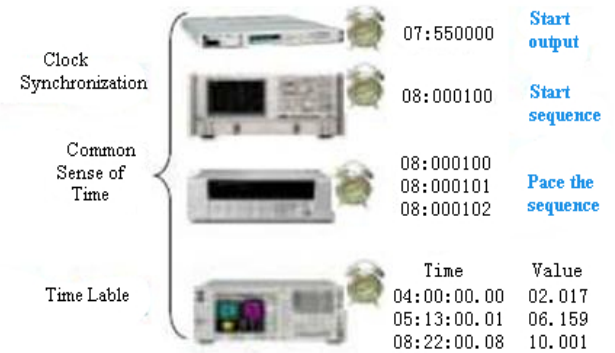

Figure 2: Timing configuration for LXI devices.

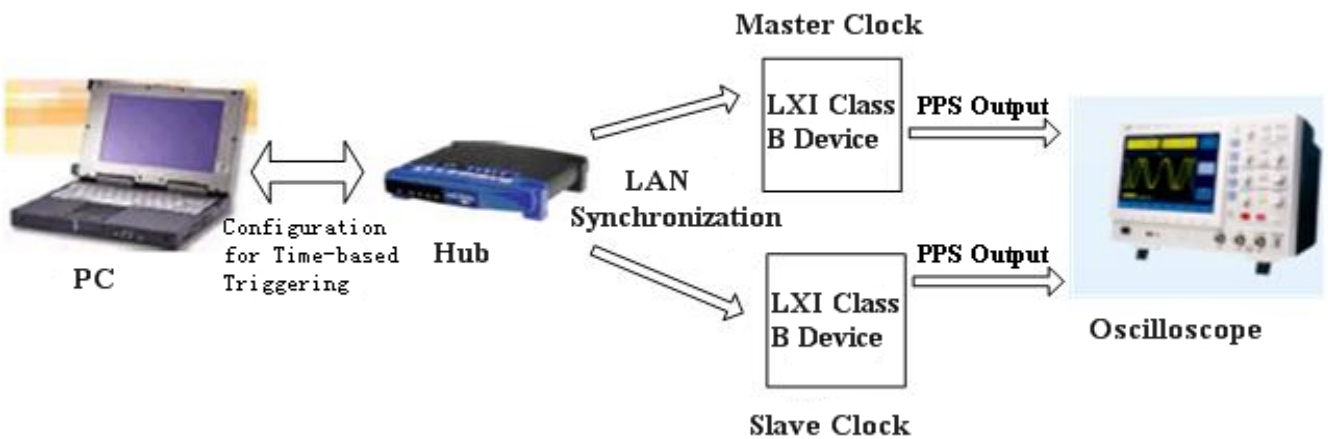

Figure 3: Lxi Class B Instruments Clock Synchronization Performance Test.

Lxi Class B Devices Synchronization Test

In many occasions, synchronization and triggering tests are critically necessary for LXI Class A and B devices since the high requirements for synchronization and triggering precision. As referred in Section 3.2 of the LXI Device Specification Revision 1.4, a Pulse-Per-Second (PPS) output shall be available on all LXI Devices implementing IEEE 1588, which is used for network Clock Synchronization Performance Test. How LXI instruments are used for test are connected is shown in fig. 3 and the two instruments shall be configured by the host PC. Then two instruments start to run IEEE 1588 Best Master Clock (BMC) to determine which one should be selected as the master, while the other one as slave. After that, two instruments synchronize to another based on the specification. Once accomplishing synchronization, the clock error of two instruments' PPS outputs will be shown through oscilloscope, and the error should be a statistic value of repeated measurements.

The clock synchronization of two LXI Class B instruments doesn't mean the real implementation of the synchronization. As shown in Fig. 4, two signal sources intend to generate two signals synchronously via Time-based Triggering. Despite the synchronization of these two signal sources clock, the delay between receiving a trigger signal and outputting waveform varies differently, which will cause the delay between two signals' waveform.

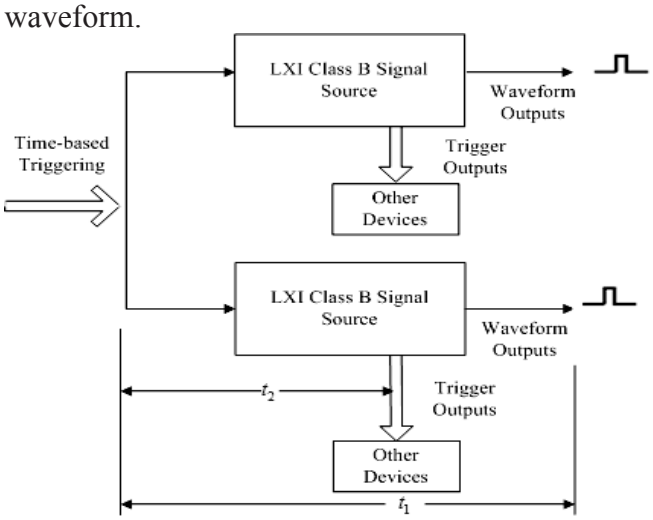

Figure 4: Meanings of Two Response Times In LXI Class B Devices

Therefore, when engaged in the research of system synchronization, other two time factors should be taken into consideration. The first one is Trigger Response Times, and another one is Trigger Output Response Times. As referred in Section 3.5.1.3 of the LXI Device Specification Revision 1.4, all LXI Devices shall specify Trigger Response Times. Take LXI Class B Signal Source for example, Trigger Response Times refers to t_1 (shown in Fig. 4), the time interval between the generation of Time-based Triggering and the waveform output. As is required, information including the minimum, maximum, and typical value of t_1(exclusive of LAN latencies and other timing effects that are external to the LXI Device itself) shall be given by manufacturers in the published specification. For response times that are probabilistic in nature, the minimum and maximum response times of t_1 shall be specified with a 95% confidence. If the response time is unknown or cannot be determined, the manufacturers shall explicitly state that the time is unknown.

Since the value of t_1 differs between LXI Devices, LAN Clock Synchronization can only ensure these two instruments will be triggered punctually, but it can't guarantee the two signal sources will output waveforms simultaneously. If two signal waveforms are relevant and there is a strict phase requirement on them, test results will be seriously influenced by the asynchronous outputs of these signal waveforms. LXI Class B Devices synchronization can achieve sub microsecond or nanosecond level precision, the range and error of t_1 should be given by manufactures and the value, t_1 can be eliminated as system error for calibration. More flexible way is to add a delay module to each instrument, so t_1 can be configured by the user. For example, t_1 can be configured, ranging from 20ns to 2s .Trigger Response Times t_1 of two signal sources can be configured to the same by the user when the clock synchronization of the two instruments is accomplished, therefore it can ensure waveforms will be output simultaneously from the two signal sources.

Though Trigger Response Times really matters, it's pretty inconvenient to measure its value for some instruments because their instruments

types vary a lot. For example, oscilloscope is used for data acquisition, and it has no response signal outputs. Therefore, another time factor Trigger Output Response Times shall be specified as required in LXI Specification. Trigger Output Response Times refers to t_2 (shown in Fig. 4). It's recommended in LXI Specification that a trigger output shall be available so that LXI Device could output a trigger signal via the trigger output when it's triggered by each of the possible triggering methods. So t_2 is a genuine delay between generating a trigger signal and signal output. As is required, information including the minimum, maximum, and typical value of t_2 shall be given by manufacturers in the published specification. For response times that are probabilistic in nature, the minimum and maximum response times of t_2 shall be specified with a 95% confidence. If the response time is unknown or cannot be determined, the manufacturers shall explicitly state that the time is unknown.

For convenience, a delay module shall be added to each instrument by manufactures to ensure that t_2 can be configurable by the user, which is similar to t_1. So all the instruments in the automatic test system can achieve synchronization.

Lxi Class A Devices Synchronization Test

LXI Class A instruments have LXI Hardware Bus besides the features of Class B. How LXI Class A instruments hardware triggering test is performed is shown in Fig. 5. As shown in the figure, two LXI Class A signal sources are interconnected with LXI trigger bus. Once master device receiving triggering signal, slave device will be triggered by master device via LXI trigger bus, then waveform response outputs of two signal sources will be acquired by oscilloscope ,and the response outputs delay will be calculated simultaneously which indicates the time precision of LXI Hardware Bus Triggering and synchronization. Besides, response outputs delay should be a statistic value for repeated measurements. For some instruments that there are no response outputs available (e.g. oscilloscope), response outputs can be replaced by trigger outputs.

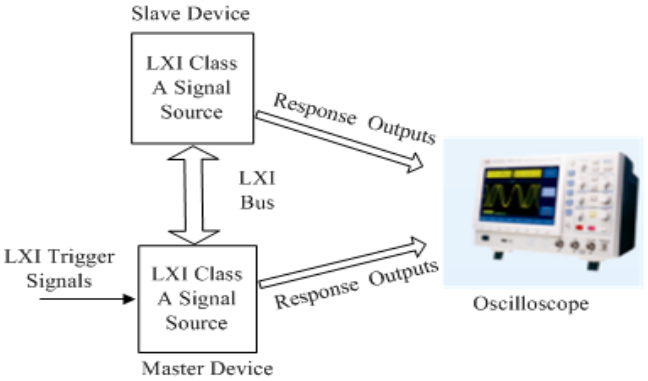

Figure5: LXI Class A Instruments Synchronization Performance Test

It can be seen that Trigger Response Times and Trigger Output Response Times should also be taken into consideration in the test. For example, it's required that synchronization of the two signal sources should achieve a precision of 5ns±5ns/m. It means the time error of outputting waveforms shall be less than ±10ns if the two signal sources are interconnected with a one-meter-length trigger bus. Since response time differs between LXI signal sources, the range and error of Trigger Response Times t_1 and Trigger Output Response Times t_2 must be taken into consideration if synchronization is expected to be nanosecond-level precision, and it can guarantee system synchronization precision through system calibration. Similar to LXI Class B devices, if t_1 and t_2 are configurable by the user, it will be more favorable to system calibration.

Lxi Instruments Synchronization and Triggering Implementation

Just take LXI Class A Logic Analyzer ES7471 designed by our center for example to analyze the implementation of LXI trigger interface. Generally, LXI instrument hardware consists of two parts: Interface Circuit and Functionality Circuit. The former is designed to implement LXI Bus synchronization and triggering functionality, and the latter for user-defined functionality. The design of Interface Circuit is shown in Fig. 6.

ARM9 (S3C2440) Core Board is selected as the hardware development platform of LXI Interface Circuit in ES7471. And the core board, the minimum ARM system consists of ARM9, Memories, Power module and so on.

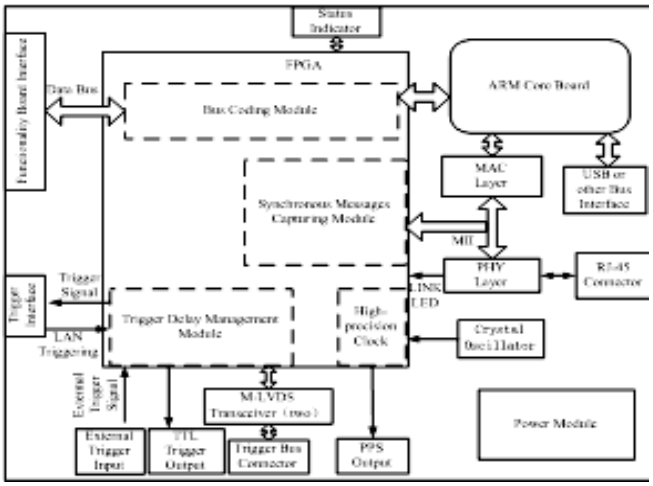

Figure6: Design of LXI Class A Logic Analyzer Interface Circuit

DM9000 is used as MAC layer chip in Ethernet Interface Circuit. DM9000 includes both MAC and PHY layer functionality. Besides, an external MII Interface is reserved. Therefore, FPGA could capture data streams which will be time stamped later from MII interface. DM9000E communicates with ARM9 via 16-bit Data Bus that interconnect both sides, and DM9000E Data Bus is compatible with ISA Bus. DP83848 is used as PHY layer chip. Other than supporting Type 10BASE-T and 100BASE-TX Ethernet, DP83848 also supports Auto-MDIX, Auto-Negotiation and other functions.

FPGA internal circuit unit mainly consists of the following modules: Synchronous Messages Capturing Module, High-precision Clock Module, Triggering and Delay Management Module, Bus Coding Module and so on.

The implementation procedure of IEEE 1588 Time-based Triggering is as following. Firstly, Synchronous Messages Capturing Module starts to accomplish the detection of half-byte data stream on MII interface, and record the time when synchronous messages pass in and out the interface. Then, High-precision Clock Module will generate high-precision IEEE 1588 time unit whose rate is adjustable and current time is modifiable. By comparing the current time with the pre-configured trigger time via Clock Comparing Unit, a trigger signal will be generated and routed to trigger instruments if the time mentioned above are equivalent. Besides, the High-precision Clock Module can also generate PPS signals, a kind of TTL signal whose rising edge is synchronous with the second's transitions of the IEEE 1588 clock. PPS output signals from different devices in the system will be compared to verify synchronization performance.

Triggering and Delay Management Module is designed to manage five modes of LXI triggering. LXI hardware triggering refers to that eight-channel M-LVDS transceiver convert eight-channel trigger signals to standard M-LVDS voltage and the process is controlled by FPGA. When trigger signals are output, they will be routed to the Trigger Bus by the transceiver via Trigger Bus Connector. By contraries, the transceiver will receive eight-channel M-LVDS trigger signals from the Trigger Bus, therefore the functionality of triggering the interface via the Trigger Bus could be implemented. Two types of Trigger Bus Connector are recommended in LXI Specification: single connector and dual connector, but here dual connector Molex 83619-9011 is selected.

LXI Event Message Triggering is implemented with the combination of software and hardware. Firstly, Logic Analyzer receives an LAN data packet containing triggering information via socket. Upon receipt of the LAN data packet, the instrument will decode it, and then hardware will be configured to trigger the instrument. If the instrument has received other trigger signals, an interrupt signal will be generated from the hardware and an LAN data packet will be routed to trigger other instruments by the software upon receipt of the interrupt signal.

Besides the implementation of five modes of LXI triggering, Trigger Output Response Times is also given in Logic Analyzer and it ranges from 24ns to 29ns. It means that the total response time between receiving triggers and outputting trigger signals on the rear of the Logic Analyzer is about 24~29ns. Since the Logic Analyzer is an instrument for data acquisition, no Trigger Response Times is given.

A delay module has also been added to FPGA, so trigger delay is user-configurable and it's about 0~1 second. If the delay is configured as 0, it means Trigger Response Times is 24-29ns. If it's set to t, then Trigger Response Times ranges from (24+t) ns to (29+t) ns.

Lxi Instruments Clock Synchronization Test

IEEE 1588 Clock Synchronization tests have been carried out on LXI Class A Logic Analyzer ES7471. The testing conditions are as following: Temperature:15C; Equipment: an Agilent oscilloscope (MSO6102A), two ES7471, two BNC connector wires, an internet cable (1.5 meter long);Testing approach: Firstly, two Logic Analyzer are interconnected with the internet cable, then PPS outputs of these two Logic Analyzer shall be connected to two input channels of MSO6102A respectively (as shown in Fig. 7). What follows is to start these two Logic Analyzers after completing above steps, then two PPS outputs will send out a square waveform per second respectively and two square waveforms will be captured by oscilloscope. Afterwards, IEEE 1588 synchronization program should be run on the two Logic Analyzers, and they will start auto-detection to determine which one should be selected as the master clock while the other as slave. During the process of clock synchronization, the time of these clocks will approximate gradually, which means rising edge of two PPS signals will approximate gradually. Synchronization precision of these two instruments can be indicated by the interval of two waveforms shown on oscilloscope. Since synchronization precision is a statistic value of repeated measurements, 100sets of measurement data are given in the test (shown in Table 1 and the unit is ns) and the average value is -2.63ns, its standard deviation is 19.5890ns.

Figure7: LXI Class A Logic Analyzer Synchronization Test

Table 1: Clock Synchronization Test Results

Times	Precision (ns)	Times	Precision (ns)
1	-6	51	4
2	-3	52	11
3	1	53	6
4	20	54	10
5	5	55	27
6	6	56	10
7	-9	57	7
8	-5	58	39
9	-18	59	40
10	-3	60	-12
11	6	61	4
12	16	62	-9
13	3	63	-25
14	11	64	8
15	9	65	-32
16	3	66	-4
17	1	67	-11
18	-5	68	-10
19	8	69	-5
20	16	70	27
21	35	71	-28
22	5	72	-10
23	-8	73	-5
24	-11	74	27
25	-19	75	-28
26	-43	76	-10
27	-15	77	24
28	-10	78	4
29	-16	79	-5
30	-29	80	-8
31	-20	81	-38
32	-7	82	-14
33	6	83	-13
34	-26	84	-17
35	-6	85	-6
36	-19	86	-35
37	-10	87	4
38	2	88	-7
39	-10	89	-65
40	-11	90	-15
41	-46	91	-3
42	-30	92	-15
43	9	93	12
44	-27	94	16
45	-22	95	-9
46	26	96	16
47	24	97	20
48	63	98	-7
49	16	99	-8
50	19	100	-1

Conclusion

The results show that two instruments can synchronize to each other with nanosecond level precision. The research has designed synchronization and triggering interface successfully, which meets LXI specification and IEEE1588 specification. And it will promote the development of the LXI synchronization and triggering technology and application.

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